

# SSC32210

## Monolithic Pressure Sensor Interface

### Features

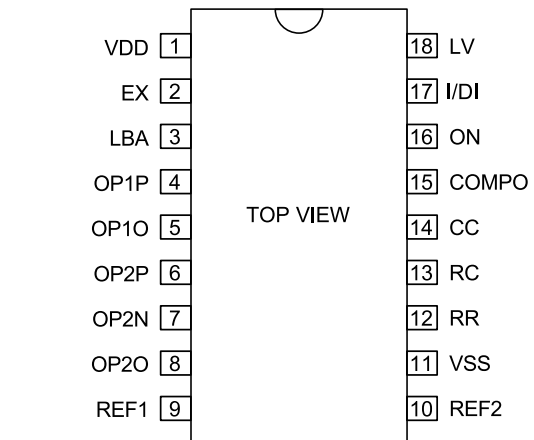
- Dual-Slope A/D Converting
- Low Power : 0.9mW
- Low Operating Voltage : 2.4
- 0.5 $\mu$ A shutdown current
- High Power-Supply Rejection
- Noise Tolerant
- Adjustable Low-Battery Detector
- Low Cost

### General Description

The SSC32210 is a high performance, very low power, front-end analog processor chip. All necessary active devices are contained on a single chip, including operational amplifier, comparators, low battery detector, switched voltage source and charge/discharge control circuitry.

The SCC32210 is designed specifically to drive a piezo- resistive pressure sensor and providing the analog architecture of dual-slope converting to operate from the control bus of a wide variety of microprocessor.

The input stage consists of a high impedance buffer to achieve stable bias current with varying input voltage. A built-in low noise amplifier is used for

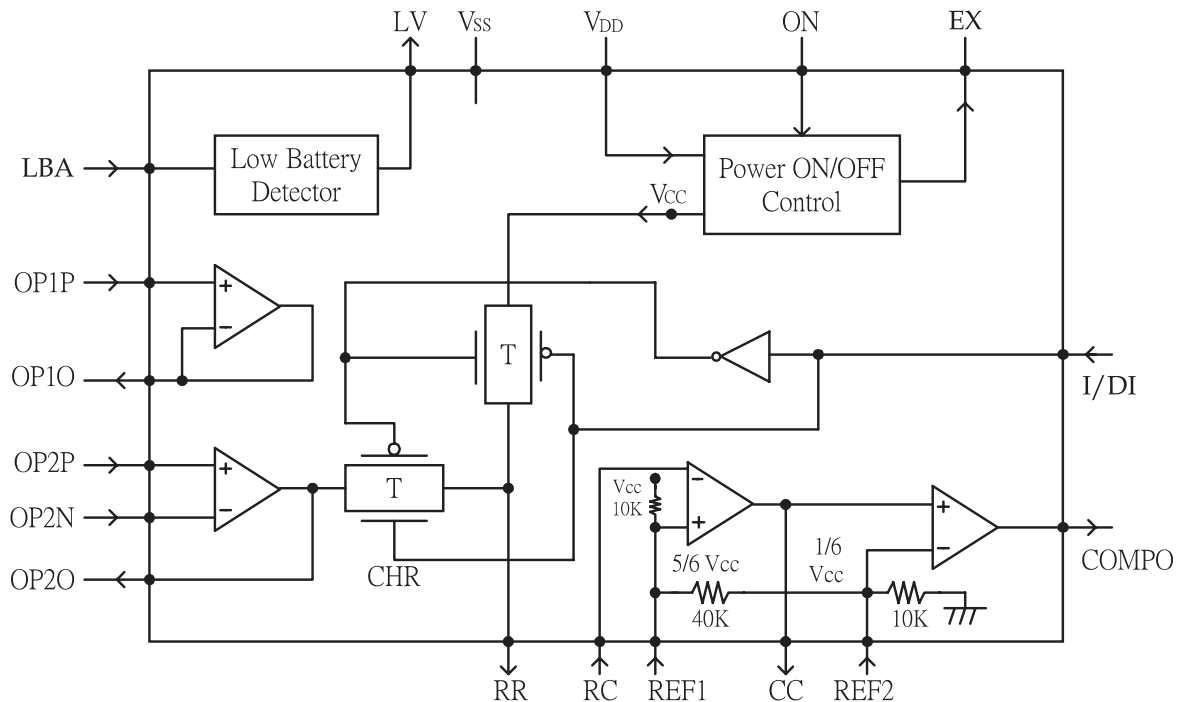


**Pin Assignment**

achieving high level output from the buffer. In operation, the unknown amplified signal voltage is integrated during a certain time, then de-integrates to a known reference voltage and measures the amount of time required to bring the integration back to its original value (the value before the signal integrate phase).

When charged by a constant current the voltage on the external capacitor is a linear function of time and can be used to connect the input voltage being measured to the time as determined by a digital counter.

## Block Diagram



## Functional Descriptions

### 1. LBA/LV

SSC32210 has a built-in low-battery detector, of which the LBA is low battery adjustment pin, where an external resistor-divider is used to set the desired trip voltage. When the supply voltage is below the reference voltage, the LV pin (a CMOS output) goes low.

### 2. Operational Amplifier OP1

OP1 is configured as a voltage follower internally to provide low impedance at the input of OP2 to preserve good common mode rejection.

### 3. Operational Amplifier OP2

OP2 is configured as non-inverting amplifier. This provides a correcting way to the low level uncalibrated sensor and achieves a high-level output signal.

### 4. Transmission Gates & Integrator

The transmission gate consists of digitally controlled analog switches implanted in 0.5 micron CMOS technology. They are controlled externally and feature low "on" resistance and low "off" leakages to configure the analog path for charging and discharging on the integrating capacitor without distortion.

Based on proper integrating interval, the integrating resistor and capacitor should be

selected to remain in linear region and give maximum voltage swing. An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors, while 0.22 $\mu$ f polypropylene capacitor gives good result at affordable cost.

#### **5. Integrate Control I/DI**

When the I/DI goes high, SSC32210 will enter to signal integrate phase. The current  $I_{CH} = (V_{REF1} - V_{IN})/R$  that is proportional to the amplified signal will charge the integrating capacitor C1. The signal continues to be integrated for a predicted time interval T1 that is determined by the user's program.

When I/DI goes low, it will enter to reference integrate (de-integrate) phase. At the beginning of this phase, the integrator input is switched from  $V_{IN}$  to  $V_{CC}$ . The polarity of the reference voltage will be opposite of the input signal, and the integration capacitor will discharge at a rate proportional to  $(V_{CC} - V_{REF1})/R$ .

#### **6. COMPO**

In de-integrating phase, the path of integrator is switched to reference voltage and the counter of controlling processor is initially reset to zero. The control logic will enable the counter in the end of integrate phase. Thus, the output of counter will keep incrementing and stop counting as long as the comparator output COMPO goes low.

The counter output is proportional to the measured signal and can be converted to digital data through external processor.

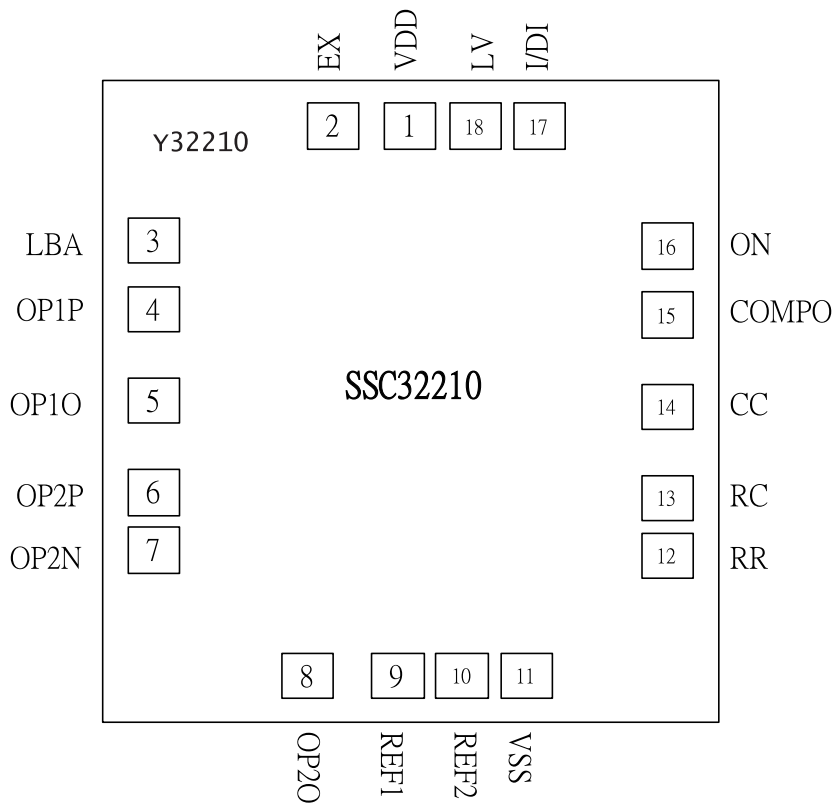
#### **7. ON**

When ON pin is low, the SSC32210 enter shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference). The supply current drops to less than 2  $\mu$ A. The ON pin is a CMOS input. Connect this pin to high for normal operation.

#### **8. Switched Voltage Source EX**

The EX is used for sensor excitation and controlled by ON synchronously. The out voltage of EX is ratiometric to the supply voltage, and the current output is 10mA typically.

## PAD Assignment



Die Size : 1150 x 1260  $\mu$ M  
Substrate Bias: Negative Supply

Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	VDD	455.8	1077.0	10	REF2	617.2	53.4
2	EX	330.3	1077.0	11	VSS	728	53.9
3	LBA	52.1	840.2	12	RR	965.7	289.8
4	OP1P	46.5	719.2	13	RC	966.9	406.9
5	OP1O	56.7	579.2	14	CC	963.3	552.7
6	OP2P	56.8	403.0	15	COMPO	962.6	700.4
7	OP2N	52.3	286.4	16	ON	962.4	822.3
8	OP2O	335.2	53.0	17	I/DI	683.4	1078.4
9	REF1	508.7	58.1	18	LV	572.6	1074.7

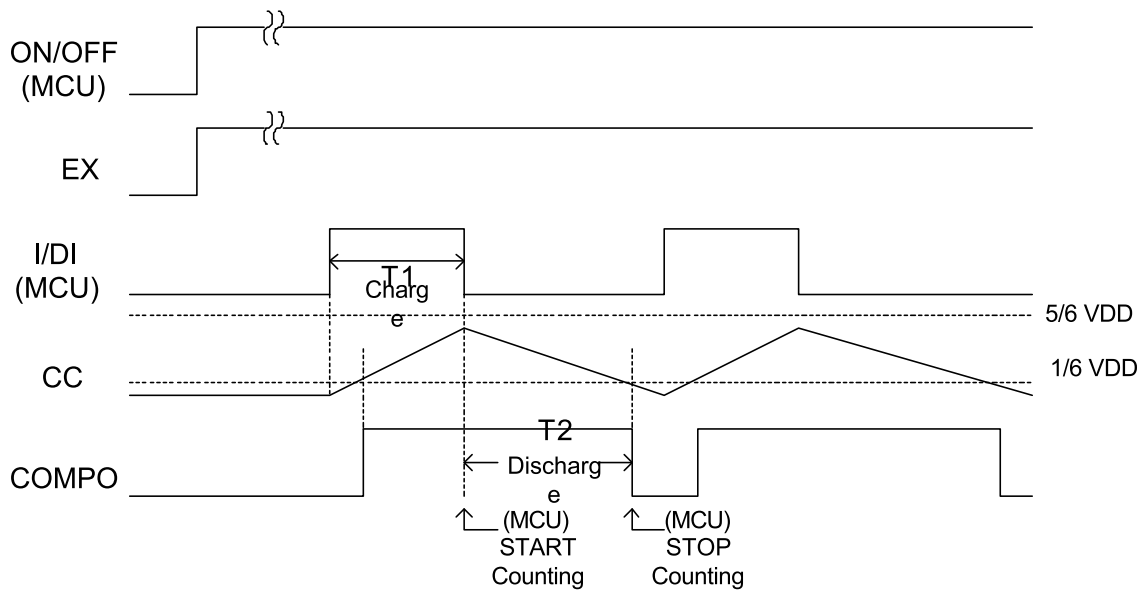
### **Pad Description**

Pad No	Pad Name	I/O	Description
1	VDD	-	Positive power supply
2	EX	O	Sensor excitation
3	LBA	I	Low-battery adjustment
4	OP1P	I	Differential input “ - “ , positive input of the 1 <sup>st</sup> OPA
5	OP1O	I/O	The 1 <sup>st</sup> stage of OPA voltage follow end
6	OP2P	I	Differential input “ + “ , positive input of the 2 <sup>nd</sup> OPA
7	OP2N	I	Negative input of the 2 <sup>nd</sup> stage of OPA
8	OP2O	I	Output of the 2 <sup>nd</sup> stage of OPA.
9	REF1	I	Input of reference voltage trimming, positive input of 3 <sup>rd</sup> OPA
12	REF2	I	Input of reference voltage trimming, negative input of 4 <sup>th</sup> OPA
13	VSS	-	Negative power supply
14	RR	I	The terminal of integrating resistor
15	RC	I	The terminal of integrating capacitor and resistor, negative input of the 3 <sup>rd</sup> stage of OPA
16	CC	O	The terminal of integrating capacitor, output of the 3 <sup>rd</sup> stage of OPA
17	COMPO	O	The output of built-in comparator
18	ON	I	System power supply control; Hi=ON, Low=shutdown
19	I/DI	I	The ADC charge and discharge control; Hi=Charge, Low=Discharge
20	LV	O	Low-battery detector output. For battery low, the output goes low

### **Electrical Characteristics**

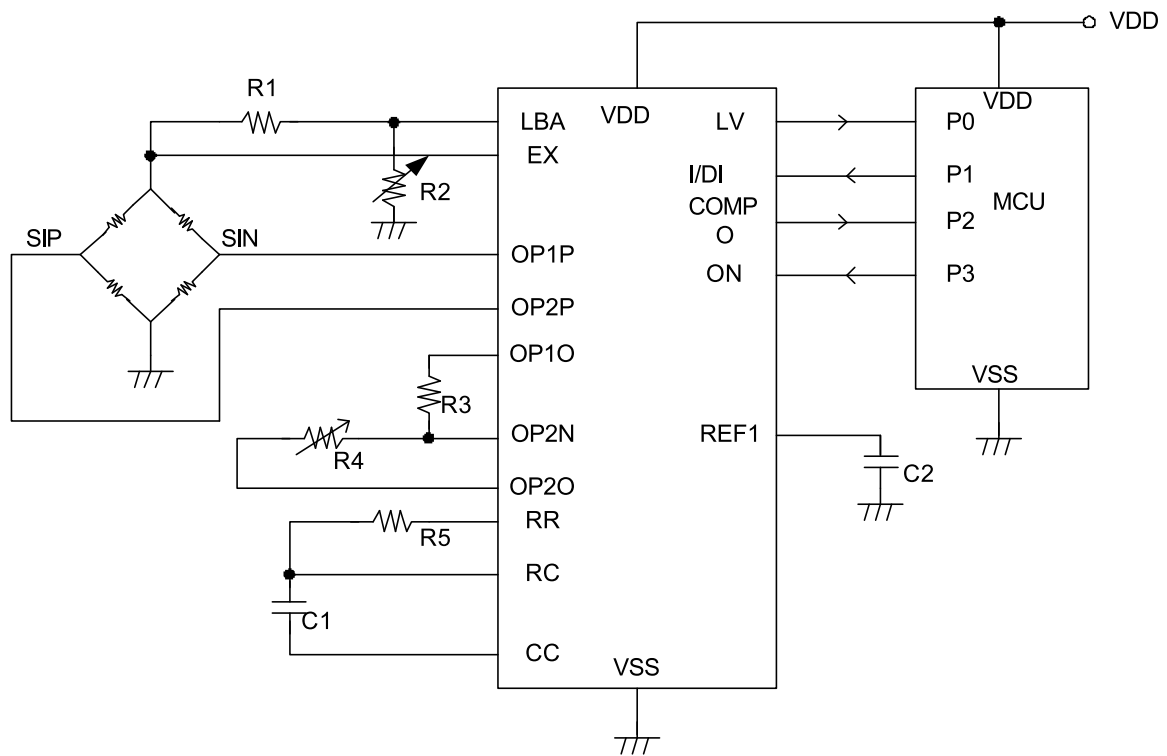
Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
V <sub>DD</sub>	Operation Voltage			2.4	3.0	5.2	V
I <sub>DD</sub>	Operation Current	3V	With Loading	-	300	500	uA
I <sub>STB</sub>	Standby Current	3V	ON=off	-	0.5	2	uA
I <sub>EX</sub>	Source Current	3V	ON = 1	-	10	12	mA
I <sub>COMPO</sub>	Sink Current	3V	ON = 1	-	1.0	1.1	mA

## Application Notes



T1: Integrate Time (preset in programming)

T2: De-Integrat Time (propotional to the measured signal)



## Typical Programming Flow

